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EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 09/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/730,120	SHIBATA, KOHSAKU	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,18,19,22 and 23* is/are rejected.

7)☒ Claim(s) *14-17,20 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *March 9, 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-23 of the application have been examined.

Foreign Priority

2. Acknowledgment is made of applicant's claim for foreign priority based on an application 2002-360362 filed in Japan on December 12, 2002. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. Acknowledgment is made of the information disclosure statements filed on September 9, 2004 together with a list of patents. The patents have been considered.

Drawings

4. The drawings submitted on December 9, 2003 are accepted.

Specification

5. The disclosure is objected to because of the following informalities:

Page 3, Line 30, "instructions that is included" appears to be incorrect and it appears that it should be "instructions that is included".

Page 4, Line 8, "an acception unit" appears to be incorrect and it appears that it should be "an acceptation unit".

Page 17, Line 12, "a branch are issued" appears to be incorrect and it appears that it should be "branches are issued".

Page 22, Lines 3-4, "resource information update unit 33" appears to be incorrect as Fig. 12 shows "resource information change unit 33".

Page 22, Line 5, "instruction execution status storage unit 25" appears to be incorrect as Fig. 12 shows "instruction execution condition storage unit 25".

Page 31, Line 15, "instruction execution status storage unit 25" appears to be incorrect as Fig. 12 shows "instruction execution condition storage unit 25".

Page 31, Line 23, "the pipeline status display unit 24" appears to be incorrect as Fig. 12 shows "the pipeline condition display unit 24".

Page 31, Line 30, "stored contents is used" appears to be incorrect and it appears that it should be "stored contents are used".

Page 31, Lines 29-32, "The stored contents is used for reconstructing the register data before executing the respective instructions included in the group after executing the group instructions" is not understood.

Page 36, Line 17, "instructions has been surely stored" appears to be incorrect and it appears that it should be "instructions have been surely stored".

Page 38, Line 6, "outputted contents does not need to be interpolated" appears to be incorrect and it appears that it should be "outputted contents do not need to be interpolated".

Page 42, Line 21, "The simulation control unit 34 do not judge" appears to be incorrect and it appears that it should be "The simulation control unit 34 does not judge".

Appropriate corrections are required.

Claim Objections

6. The following is a quotation of 37 C.F.R § 1.75 (d)(1):

> The claim or claims must conform to the invention as set forth in the remainder of the specification and terms and phrases in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description.

7. Claim 7 is objected to because of the following informalities:

Claim 1, Line 6, "an acception unit" appears to be incorrect and it appears that it should be "an acceptation unit".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claim 21 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 21 states in part, " wherein the reconstruction apparatus further generates data of resources " on Line 2-3 of the claim. There is insufficient antecedent basis for this limitation in the claim. Claim 20 refers to "the reconstruction unit" and not "the reconstruction apparatus".

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

11. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. Claims 1-9, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Matsumoto et al.** (U.S. Patent Application 2003/0204819) in view of **Moller et al.** (U.S. Patent 6,826,522).

12.1 **Matsumoto et al.** teaches method of generating development environment for developing system LSI and medium which stores program therefor. Specifically, as per claim 1, **Matsumoto et al.** teaches a simulation apparatus that is intended for a very long instruction word processor (Page 1, Para 0011, L3-14; Page 6, Para 0128, L8-13; Page 8, Para 0157, L1-3; Para 0158, L4-5; Para 01259, L8-12; Para 0160).

Matsumoto et al. teaches pipeline instruction execution (Page 13, Para 0308; Para 0315, Para 0321, Para 0324). **Matsumoto et al.** does not expressly teach a first simulation unit operable to simulate execution of a group of instructions to be executed simultaneously. **Moller et al.** teaches a first simulation unit operable to simulate execution of a group of instructions to be executed simultaneously (Abstract, L2-3 and L6-16; Fig. 4; CL1, L20-22; CL1, L51-59; CL6, L31-34). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the simulation apparatus of **Matsumoto et al.** with the simulation apparatus of **Moller et al.** that included a first simulation unit operable to simulate execution of a group of instructions to be executed simultaneously, because in a pipelined computer, instructions pass through various stages in such a way that all of the stages may be in use simultaneously, each performing the tasks associated with different instructions (CL1, L51-54; Fig. 4).

Matsumoto et al. teaches generation of a simulator that executes instruction operations (Page 5, Para 0101; Page 6, Para 0128, L1-5; Page7, Para 0128, L2-8). **Matsumoto et al.** does not expressly teach a second simulation unit operable to generate a simulation result of the group of instructions on an instruction-by-instruction basis based on a simulation result generated by the first simulation unit. **Moller et al.** teaches a second simulation unit operable to generate a simulation result of the group of instructions on an instruction-by-instruction basis based on a simulation result generated by the first simulation unit (CL6, L44-62; Fig. 5 and Fig. 6; CL8, L65-66).

12.2 As per claim 2, **Matsumoto et al.** and **Moller et al.** teach the simulation apparatus of claim 1. **Matsumoto et al.** does not expressly teach that the second simulation unit generates a simulation result by undoing a simulation of an instruction included in a group of instructions that has just been simulated by the first simulation unit. **Moller et al.** teaches that the second simulation unit generates a simulation result by undoing a simulation of an instruction included in a group of instructions that has just been simulated by the first simulation unit (CL6, L44-62; Fig. 5 and Fig. 6; CL8, L65-66).

Per claim 3: **Matsumoto et al.** teaches a display control unit operable to control a display unit to display the simulation result generated by the second simulation unit (Page 5, Para 0104, L1-3).

12.3 As per claim 4, **Matsumoto et al.** and **Moller et al.** teach the simulation apparatus of claim 2. **Matsumoto et al.** teaches a judgment unit operable to judge whether an instruction that satisfies a break condition is included in the group of instructions that has just been simulated by the first simulation unit or not (Page 5, Para 0108, L1-2, L11-13 and L16-18);

an indication unit operable to indicate that the first simulation unit simulates execution of a next group of instructions when it is judged that no instruction satisfying the break condition is included (Page 5, Para 0108);

a determination unit operable to determine an instruction as a stop instruction when it is judged that the instruction satisfying the break condition is included (Page 5, Para 0108, L1-2, L11-13 and L16-18); and

a generation unit operable to generate a simulation result by undoing simulations of the stop instruction and the following instructions in the group of instructions that have just been simulated (Page 5, Para 0108).

12.4 As per claim 5, **Matsumoto et al.** and **Moller et al.** teach the simulation apparatus of claim 1. **Matsumoto et al.** teaches the first simulation unit is intended for a pipeline processor (Page 13, Para 0308; Para 0315, Para 0321, Para 0324). **Matsumoto et al.** does not expressly teach that the first simulation unit is intended for a pipeline processor that executes a plurality of instructions simultaneously. **Moller et al.** teaches that the first simulation unit is intended for a pipeline processor that executes a plurality of instructions simultaneously (Abstract, L2-3 and L6-16; Fig. 4; CL1, L20-22; CL1, L51-59; CL6, L31-34).

Matsumoto et al. does not expressly teach a display image generation unit operable to generate a display image showing instructions that are included in a pipeline based on simulation results generated by the first simulation unit and the second simulation unit. **Moller et al.** teaches a display image generation unit operable to generate a display image showing instructions that are included in a pipeline based on simulation results generated by the first simulation unit and the second simulation unit (Fig. 4; CL6, L35-41).

12.5 As per claim 6, **Matsumoto et al.** and **Moller et al.** teach the simulation apparatus of claim 5. **Matsumoto et al.** does not expressly teach that the display image contains representation of an instruction that is included in every stage of the pipeline. **Moller et al.** teaches that the display image contains representation of an instruction that is included in every stage of the pipeline (Fig. 4; CL6, L35-41).

12.6 As per claim 7, **Matsumoto et al.** and **Moller et al.** teach the simulation apparatus of claim 1. **Matsumoto et al.** teaches that an acception unit operable to accept a user operation that indicates one of a step execution performed on an instruction-by-instruction basis and a step execution performed on a cycle-by-cycle basis (Page 7, Para 0128, L2-5; Para 0129); and

a display image generation unit operable to generate a display image that shows a simulation result generated on an instruction-by-instruction basis by the second simulation unit when a user operation that indicates a step execution performed on an instruction-by-instruction basis is accepted (Page 5, Para 0104, L1-3), and to generate a display image that shows a simulation result generated on a cycle-by-cycle basis by the first simulation unit when a user

operation that indicates a step execution performed on a cycle-by-cycle basis is accepted (Page 5, Para 0104, L1-3).

Matsumoto et al. does not expressly teach that the first simulation unit simulates, on a cycle-by-cycle basis, operations of a pipeline processor that executes a plurality of instructions simultaneously. **Moller et al.** teaches that the first simulation unit simulates, on a cycle-by-cycle basis, operations of a pipeline processor that executes a plurality of instructions simultaneously (Abstract, L2-3 and L6-16; Fig. 4; CL1, L20-22; CL1, L51-59; CL6, L31-34).

12.7 As per claims 8 and 9, **Matsumoto et al.** and **Moller et al.** teach the simulation apparatus of claim 7. **Matsumoto et al.** does not expressly teach that the display image contains representation of each instruction that is included in a pipeline; and the display image contains representation of instructions that is included in every stage of a pipeline. **Moller et al.** teaches that the display image contains representation of each instruction that is included in a pipeline; and the display image contains representation of instructions that is included in every stage of a pipeline (Fig. 4; CL6, L35-41).

12.8 As per Claims 22 and 23, these are rejected based on the same reasoning as Claim 1, supra. Claims 22 and 23 are simulation method and program claims reciting the same limitations as Claim 1, as taught throughout by **Matsumoto et al.** and **Moller et al.**

13. Claims 10-13 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Matsumoto et al.** (U.S. Patent Application 2003/0204819) in view of **Moller et al.** (U.S. Patent 6,826,522), and further in view of **Ussery et al.** (U.S. Patent Application 2001/0025363).

13.1 As per claim 10, **Matsumoto et al.** and **Moller et al.** teach the simulation apparatus of claim 1. **Matsumoto et al.** teaches that the first simulation unit includes a hold unit operable to hold first data showing resources of the very long instruction word processor (Page 13, Para 0315; Page 8, Para 0158 and Para 0160).

Matsumoto et al. and **Moller et al.** do not expressly teach that the first simulation unit includes a storage unit operable to store a copy of the first data in the memory unit as second data. **Ussery et al.** teaches that the first simulation unit includes a storage unit operable to store a copy of the first data in the memory unit as second data (Page 2, Para 0015 and Para 0022). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the simulation apparatus of **Matsumoto et al.** and **Moller et al.** with the simulation apparatus of **Ussery et al.** that included the first simulation unit including a storage unit operable to store a copy of the first data in the memory unit as second data, because that would allow the designer to configure the multi-processor systems such as the configurable VLIW architectures (Page 1, Para 0013, L1-3; Para 0008, L9-11).

Matsumoto et al. and **Ussery et al.** do not expressly teach a first simulator that updates the first data by simulating an execution of a single group of instructions after storing the copy. **Moller et al.** teaches a first simulator that updates the first data by

simulating an execution of a single group of instructions after storing the copy (Abstract, L2-3 and L6-16; Fig. 4; CL1, L20-22; CL1, L51-59; CL6, L31-34).

Matsumoto et al. and **Ussery et al.** do not expressly teach that the second simulation unit obtains simulation results of the group of instructions on an instruction-by-instruction basis based on the first data and the second data. **Moller et al.** teaches that the second simulation unit obtains simulation results of the group of instructions on an instruction-by-instruction basis based on the first data and the second data (CL6, L44-62; Fig. 5 and Fig. 6; CL8, L65-66).

13.2 As per claim 11, **Matsumoto et al., Moller et al.** and **Ussery et al.** teach simulation apparatus of claim 10. **Matsumoto et al.** and **Moller et al.** do not expressly teach that the storage unit stores data of a register set in the memory unit as the second data, and the second simulation unit reconstructs data. **Ussery et al.** teaches that the storage unit stores data of a register set in the memory unit as the second data (Page 2, Para 0015 and Para 0022), and the second simulation unit reconstructs data (Page 3, Para 0026, L1-3).

Matsumoto et al. and **Ussery et al.** do not expressly teach that the second simulation unit reconstructs data of the resource before executing a simulation of the instruction of the group of instructions on an instruction-by-instruction basis. **Moller et al.** teaches that the second simulation unit reconstructs data of the resource before executing a simulation of the instruction of the group of instructions on an instruction-by-instruction basis (CL6, L44-62; Fig. 5 and Fig. 6; CL8, L65-66).

13.3 As per claim 12, **Matsumoto et al., Moller et al.** and **Ussery et al.** teach simulation apparatus of claim 11. **Matsumoto et al.** and **Moller et al.** do not expressly teach that the storage unit further stores memory data before memory writing in the hold unit in a way that said memory data is contained in the second data when a memory write instruction is included in the group of instructions. **Ussery et al.** teaches that the storage unit further stores memory data before memory writing in the hold unit in a way that said memory data is contained in the second data when a memory write instruction is included in the group of instructions (Page 2, Para 0015 and Para 0022).

13.4 As per claim 13, **Matsumoto et al., Moller et al.** and **Ussery et al.** teach simulation apparatus of claim 10. **Matsumoto et al.** teaches a judgment unit operable to judge whether an instruction that satisfies a break condition is included in the group of instructions that has just been simulated by the first simulation unit or not (Page 5, Para 0108, L1-2, L11-13 and L16-18);

an indication unit operable to indicate that the first simulation unit simulates execution of a next group of instructions when it is judged that no instruction satisfying the break condition is included (Page 5, Para 0108); and

a determination unit operable to determine an instruction that satisfies the break condition as a stop instruction when it is judged that the instruction satisfying the break condition is included (Page 5, Para 0108, L1-2, L11-13 and L16-18).

13.5 As per claim 18, **Matsumoto et al., Moller et al.** and **Ussery et al.** teach simulation apparatus of claim 10. **Matsumoto et al.** and **Ussery et al.** do not expressly teach that the first

simulator simulates execution of the group of instructions on a cycle-by-cycle basis of pipeline processing , the first simulator being intended for the very long instruction word processor that executes the pipeline processing, and the simulation apparatus further counts the number of execution cycles in the simulation for every group of instructions. **Moller et al.** teaches that the first simulator simulates execution of the group of instructions on a cycle-by-cycle basis of pipeline processing (Abstract, L2-3 and L6-16; Fig. 4; CL1, L20-22; CL1, L51-59; CL6, L31-34), the first simulator being intended for the very long instruction word processor that executes the pipeline processing (Abstract, L2-3 and L6-16; Fig. 4; CL1, L20-22; CL1, L51-59; CL6, L31-34), and the simulation apparatus further counts the number of execution cycles in the simulation for every group of instructions (Fig. 4; CL6, L35-41).

14. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Matsumoto et al.** (U.S. Patent Application 2003/0204819) in view of **Moller et al.** (U.S. Patent 6,826,522), and further in view of **Ussery et al.** (U.S. Patent Application 2001/0025363) and **Miyake et al.** (U.S. Patent 6,681,280).

14.1 As per claim 19, **Matsumoto et al., Moller et al.** and **Ussery et al.** teach simulation apparatus of claim 18. **Matsumoto et al., Moller et al.** and **Ussery et al.** do not expressly teach that the very long instruction word processor has a cancellation unit for canceling execution of an instruction in a plurality of instructions to be executed simultaneously, and the first simulator simulates the cancellation unit. **Miyake et al.** teaches that the very long instruction word processor has a cancellation unit for canceling execution of an instruction in a plurality of

instructions to be executed simultaneously, and the first simulator simulates the cancellation unit (CL8, L1-6). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the simulation apparatus of **Matsumoto et al., Moller et al.** and **Ussery et al.** with the simulation apparatus of **Miyake et al.** that included the very long instruction word processor having a cancellation unit for canceling execution of an instruction in a plurality of instructions to be executed simultaneously, and the first simulator simulating the cancellation unit, because that would allow simulating an interrupt control apparatus having break interrupt function for interrupting the execution of a program (CL1, L10-14).

Allowable Subject Matter

15. Claims 14-17 and 20-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez, can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K. Thangavelu
Art Unit 2123
September 10, 2006